REMARKS

Claims 1-11 are pending in the above-identified application. Claims 1, 3, 8, and 9 are independent.

Objections

The Specification and claims 8 and 9 have been objected to for use of the word "outputs." Accordingly, Applicant has amended the Specification and claims to replace "outputs" with "output" as recommended in the Office Action.

Claim Rejection – 35 U.S.C. 112

Claims 3-11 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The Office Action alleges that it is unclear whether claims 3-7 are directed to a device or a method. The Office Action alleges that it is unclear whether claims 8-11 are directed to a storage device, testing method or testing device.

Applicant has amended claims 8 and 9 to recite that the claimed steps are of the stored program. However, Applicant traverses the rejection otherwise. Applicant submits that claims 3-7 are clearly directed to a testing method. Even though they recite components of the testing device, claims 3-7 recite steps associated with the method, beginning with the phrase "the method comprising." The same can be said about claims 8-11, which, even though they recite components of the testing device, claims 8-11 recite steps associated

with the program. Accordingly, Applicant respectfully requests that the rejection be withdrawn.

Claim Rejection – 35 U.S.C. 103; Yamagami, Paulos, Cheng

Claims 1 and 2 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagami et al. (U.S. Patent 6,121,786), Paulos et al. (U.S. Patent 6,091,350), and Cheng (U.S. Patent 6,154,041). Applicant respectfully traverses this rejection.

Summary of the Present Invention

The present invention relates to a testing device and associated testing method for a semiconductor integrated circuit (e.g., a LCD driver integrated circuit). The testing device incorporates a multiple number of D/A converters and outputs voltages at associated output terminals. Thus, the testing device examines the output voltages from the D/A converters. (See section Field of the Invention). The present invention improves over known conventional testing devices by providing highly accurate testing without the necessity of a separate reference voltage generator for each type of semiconductor tested (Specification, page 6, lines 1-6).

In order to provide improvements over conventional testers, the present invention, as for example a LCD driver testing device, is disclosed for testing m-

output voltages. In a preferred embodiment, D/A converters output a tonal voltage for n-levels of tones. Tonal voltage outputs (Y1 to Ym) are supplied in parallel to a differential amplifier module array 4. A voltage generator sequentially generates n-levels of reference voltages to be compared to the tonal voltages. A reference voltage is input to second terminals of all differential amplifiers 5 constituting the differential amplifier array module. The reference voltage generator is able to generate a multiple number of tonal voltages, in increments of Vmin, a predetermined smallest voltage step, which enables selective generation of multiple sets of reference voltages required for testing of multiple kinds of semiconductor integrated circuits.

Each differential amplifier produces an amplified output voltage which is obtained by amplifying a voltage deviation by a given ratio (see Figure 4). This amplifying process assures high precision in comparison by comparator 12. Thus, the present invention is made up of a conventional built-in comparator type tester, adding only a differential amplifier array module and a voltage generator (Specification, page 21, lines 15-18).

Differences over Yamagami, Paulos and Cheng

The Office Action alleges that Yamagami teaches the claimed invention of claim 1, except for "D/A converters as a reference voltage generator, or selectively outputting multiple sets of reference voltages." Applicant respectfully

submits that the Office Action has misinterpreted the claimed invention. As noted above in the brief summary of the invention, it is not the D/A converters that perform these functions, but rather the reference voltage generator. The D/A converters of the present invention are incorporated in the semiconductor circuit to be tested by the testing device. They output voltages which are compared to reference voltages generated by the reference voltage generator. The D/A converters do not, as stated in the Office Action, constitute reference voltage generators or selectively output multiple sets of reference voltages.

Because of the apparent misinterpretation in the Office Action, Applicant submits that even if Cheng does disclose the deficiency of Yamagami of a D/A converter, which Applicant does not concede, Cheng's teaching of a D/A converter as a reference voltage generator does not constitute the claimed multiple number of D/A converters incorporated in the semiconductor integrated circuit that output voltages to be compared with reference voltages generated from the reference voltage generator. Similarly, even if Paulos does teach D/A converters selectively outputting a range of voltages, which Applicant does not concede, it does not disclose a reference voltage generator selectively outputting multiple sets of reference voltages.

Further, Yamagami is not directed to a testing device for a semiconductor integrated circuit, but to a semiconductor integrated circuit, itself. In other words, the circuit in Yamagami does not receive output voltages from a

semiconductor integrated circuit, and much less output voltages from D/A converters, that are compared to reference voltages from a reference voltage generator of a testing device. Thus, at least for these reasons, Yamagami, Paulos, and Cheng, either alone or in combination, fail to teach all claimed elements. Accordingly, Applicant submits that the rejection fails to establish *prima facie* obviousness for claims 1 and 2. Applicant respectfully requests that the rejection be withdrawn.

Claim Rejection – 35 U.S.C. 103; Yamagami and Ueno

The Office Action alleges that Yamagami teaches all claimed elements of claims 3 and 4, except the step of calculating the difference between the reference voltage generated from the reference voltage generator of the testing device and the output voltage output from each output terminal, for all output terminals. First of all, Applicant disagrees that Yamagami teaches a testing device for a semiconductor integrated circuit. Rather, Applicant submits that Yamagami discloses a semiconductor integrated circuit. Specifically, Yamagami teaches, among other things, a semiconductor integrated circuit having a reference voltage comparator 8 that compares two reference voltages (VREF1 and VREF2; Figure 1).

The Office Action relies on Ueno for teaching the missing calculating step of Yamagami. Applicant submits that the Office Action misinterprets the

claimed invention by alleging that Ueno's disclosure of the reference voltage generating circuit 10 (e.g., column 3, lines 46-68) teaches a step of comparing the difference between a reference voltage generated from the reference voltage generator and an output voltage of a semiconductor integrated circuit. Instead, Ueno is directed to a reference voltage generating circuit 10 for use in an analog-to-digital converter. Thus, Applicant submits that Ueno does not teach calculating a difference between a reference voltage from a reference voltage generator of a testing device and an output voltage output from terminals associated with D/A converters.

Further, Ueno's reference voltage generating circuit 10 generates a reference voltage, and for example, might serve as an alternative for reference voltage generator 1 of Yamagami. However, Applicant submits that one of ordinary skill in the art would not rely on Ueno for teaching calculating a difference based on its generated reference voltage and an output from each output terminal of a semiconductor integrated circuit. Thus, Applicant submits that all claimed elements of claims 3 and 4 are not taught or suggested by Yamagami and Ueno. Accordingly, Applicant submits that the rejection fails to establish *prima facie* obviousness for claims 3 and 4. Applicant respectfully requests that the rejection be withdrawn.

CONCLUSION

In view of the above amendments and remarks, reconsideration of the various rejections and allowance of claims 1-11 is respectfully requested.

Should the Examiner have any questions concerning this application, the Examiner is invited to contact Robert W. Downs (Reg. No. 48,222) at (703) 205-8000 in the Washington, D.C. area.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicant(s) respectfully petition(s) for a one (1) month extension of time for filing a reply in connection with the present application, and the required fee of $$110.00 is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit

Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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TCB/RWD/bsh/lab
Attachment: Version with Markings to Show Changes Made

VERSION WITH MARKING TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification has been amended as follows:

The paragraph beginning on page 10, line 21, bridging page 11, line 1, has been amended as follows:

a reference voltage generator which generates a multiple number of reference voltages to be compared to each output voltage output from each of the output terminals and can selectively [outputs] output multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits;

The paragraph on page 12, lines 18-23, has been amended as follows:

a reference voltage generator which generates a multiple number of reference voltages to be compared to each output voltage output from each of the output terminals and can selectively [outputs] output multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits;

The paragraph beginning on page 22, line 12, bridging page 23, line 6, has been amended as follows:

At S3, each differential amplifier 4, based on the associated input voltage, calculates the difference between the first tonal voltage output from the

associated terminal of LCD driver LSI 1 and the expected voltage (S3) and amplifies the calculation by a given magnification (e.g., 100 times or greater) so as to produce a voltage-amplified output voltage (S4). The voltage-amplified output voltages from all amplifiers 4 are input in parallel to tester 10, in which a given voltage range has been set up (S5). In comparator 12 of tester 10, it is judged whether each voltage-amplified output voltage falls within the given voltage range (S6). In this judgment, when AND circuit 17 produces the L-level output, which means that any of the output voltages is judged to fall out of the given range, the testing operation is stopped at that point so that the LSI under test is rejected as **[**a**]** defective (S7). On the contrary, when AND circuit 17 produces the H-level output, which means that all the output voltages are judged to fall within the given voltage range, the operation goes to the next step, i.e., the test on the second tonal voltage level (S8).

The paragraph beginning on page 23, line 7, bridging page 24, line 14, has been amended as follows:

Specifically, LCD driver LSI 1 is operated so as to output the tonal voltage representing the second tone from 'm' output terminals 3 (S1). The tonal voltages output from 'm' output terminals 3 are input in parallel to associated differential amplifiers 5 through their input terminals 6, one of the two input to each differential amplifier. Voltage generator 8 is set and

controlled, as it is supplied with the predetermined digital data signal, so as to generate an expected voltage 14 corresponding to the second tonal voltage 13 in LCD driver LSI 1 under test (S2). This expected voltage is input to the other input terminal (common input terminal) 7 of each differential amplifier 5. Each differential amplifier 5, based on the associated input voltage, calculates the difference between the second tonal voltage output from the associated terminal of LCD driver LSI 1 and the expected voltage (S3(the first step)) and amplifies the calculation by a given magnification (e.g., 100 times or greater)) so as to produce a voltage-amplified output voltage (S4(the second step)). The voltage-amplified output voltages from all amplifiers 4 are input in parallel to tester 10, in which a given voltage range has been set up (S5). In comparator 12 of tester 10, it is judged whether each voltage-amplified output voltage falls within the given voltage range (S6(the third step)). In this judgment, when AND circuit 17 produces the L-level output, which means that any of the output voltages is judged to fall out of the given range, the testing operation is stopped at that point so that the LSI under test is rejected as [a] defective (S7). On the contrary, when AND circuit 17 produces the H-level output, which means that all the output voltages are judged to fall within the given voltage range, the operation goes to the next step, i.e., the test on the third tonal voltage level (S8).

IN THE CLAIMS:

The claims have been amended as follows:

8. (Amended) A storage medium for storing the program for a computer to execute a testing method for a semiconductor integrated circuits which incorporates a multiple number of D/A converters and outputs voltages from the D/A converters via associated output terminals, wherein a testing device for semiconductor integrated circuits is used which comprises:

a reference voltage generator which generates a multiple number of reference voltages to be compared to each output voltage output from each of the output terminals and can selectively [outputs] output multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits:

a multiple number of differential amplifiers, each having two input terminals, one for receiving the output voltage output from the associated output terminal and the other for receiving the reference voltage from the reference voltage generator; and

a comparator that receives the amplified output voltages from the multiple number of differential amplifiers and judges whether the amplified output voltage from each of the differential amplifiers falls within a given voltage range, wherein the reference voltage generator includes a D/A converter which receives a digital data signal different from the signals to the D/A

converters incorporated in the semiconductor integrated circuit to generate the multiple number of reference voltages and can selectively output a necessary set of reference voltages from the multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuit, in accordance with the selection of the digital data signal,

the [method] program comprising:

the first step for calculating the difference between the reference voltage generated from the reference voltage generator of the testing device and the output voltage output from each output terminal, for all the output terminals;

the second step for amplifying the values obtained from the first step; and

the third step for judging at one time whether all the amplified differential values obtained in the second step in association with respective output terminals fall within the first given voltage range, wherein even if the output from the device under test varies, the first given voltage range can be kept at constant by computing the difference between the output from the device under test and the associated reference voltage generated from the above reference voltage.

9. (Amended) A storage medium for storing the program for a computer to execute a testing method for a semiconductor integrated circuits which

incorporates a multiple number of D/A converters and outputs voltages from the D/A converters via associated output terminals, wherein a testing device for semiconductor integrated circuits is used which comprises:

a reference voltage generator which generates a multiple number of reference voltages to be compared to each output voltage output from each of the output terminals and can selectively [outputs] output multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits:

a multiple number of differential amplifiers, each having two input terminals, one for receiving the output voltage output from the associated output terminal and the other for receiving the reference voltage from the reference voltage generator: and

a comparator that receives the amplified output voltages from the multiple number of differential amplifiers and judges whether the amplified output voltage from each of the differential amplifiers falls within a given voltage range, wherein the reference voltage generator includes a D/A converter which receives a digital data signal different from the signals to the D/A converters incorporated in the semiconductor integrated circuit to generate the multiple number of reference voltages and can selectively output a necessary set of reference voltages from the multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuit, in accordance with

the selection of the digital data signal,

the [method] program comprising:

the first step for calculating the difference between the reference voltage generated from the reference voltage generator of the testing device and the output voltage output from each output terminal, for all the output terminals;

the second step for amplifying the values obtained from the first step;

the third step for judging at one time whether all the amplified differential values obtained in the second step in association with respective output terminals fall within the first given voltage range, wherein even if the output from the device under test varies, the first given voltage range can be kept at constant by computing the difference between the output from the device under test and the associated reference voltage generated from the above reference voltage;

the fourth step for decreasing the width of the first given voltage range by a multiple of the predetermined voltage width to set up a second given voltage range: and

the fifth step for judging at one time whether all the amplified differential values associated to respective output terminals falls within the second given voltage range, wherein the fourth and fifth steps are repeated until the judgment at the fifth step changes.